ChipAsic 琦璞

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ChipAsic Technology Co.,Ltd.

DAC 12BITS 25MSPS UMC55

Specification

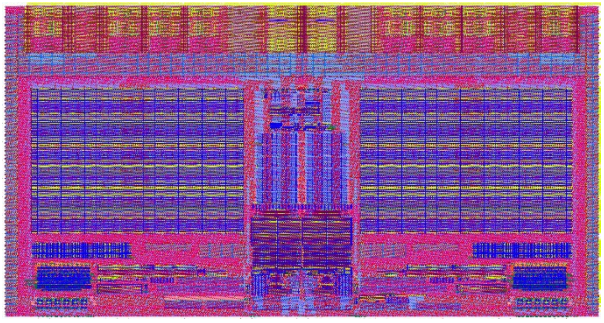
Version 0.9

Nov 01, 2022

Revision History

Ver.#	Rev.Date	Rev.By	Comment
0.9	11/01/2022	IP Team	Initial Version

Index



Product OutLine

12bits, 25Msps, Dual Channel DAC
UMC 55nm eFLASH

Status

Silicon Proven

1. Introduction

With more than 10 years of experience in developing analog IP solutions, ChipAsic offers a comprehensive portfolio of more than 40 silicon-proven Data Converter IP products consisting of analog-to-digital converters (ADCs), digital-to-analog converters (DACs), auxiliary converters, video DACs (VDACs) and analog front-ends (AFEs).

ChipAsic' strong application expertise in areas such as mobile communications, cellular IoT, and wireless connectivity, wireline communications, IF demodulation, video, imaging and multimedia results in high-quality data converter IP that helps system-on-chip (SoC) designers meet their specific design requirements.

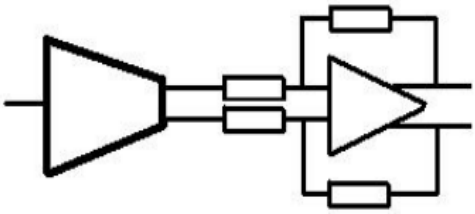
The Data Converter IP offers very high performance, high speed, ultra-low power dissipation, and small area, and supports a wide range of foundry process technologies. ChipAsic' high-quality Data Converter IP solutions have been implemented in more than 40 SoCs, giving designers confidence that they can successfully integrate high-performance analog IP into their SoCs with less risk and improved time-to-results.

The 12bits, 25Msps Dual Channels DAC is design for low power high-performance application. It is used for common Data Analog converter with 50M clock input. The IP diagram is show as following figure.

2. Tech Specs

Parameter	Symbol	Min.	Typ.	Max.	unit	Notes
Analog Voltage	VDD_A	2.97	-	3.63	V	-
Digital Voltage	VDD_D	1.08	-	1.32	V	-
Ref Voltage	VREF	1.0	-	2.0	V	-
signal Output	VAOUT	1.0	-	2.0	Vpp	-
Voltage Common Output	VCM	VDD_A	VDD_A/2	VDD_A/2	V	-
Channel Num	CH	-	2	-	-	-
Clock Input	CLK	1	-	50	MHz	duty cycle 50%±5%, Jitter(RMS)<20ps
Sample Rates	FCLK	-	25	-	MHz	-
Conversion bits	RES	-	12	-	Bits	-
Conversion Rate	FS	-	25	-	Msps	-
Effective bits	ENOB	10	-	-	bit	Fout=2MHz，CL≤10pF
Spurious-free DynamicRange	SFDR	65	-	-	dBc	Fout=2MHz, CL≤10pF
Integral Nonlinearity	INL	-4	-	4	LSB	
Differential Nonlinearity	DNL	-2	-	2	LSB	
Gain error	GAIN_E	-0.5	-	0.5	%	
Spurious-free DynamicRange	SFDR	60	-	-	dBc	Fout=10MHz, CL≤10pF
Integral Nonlinearity	INL	-4	-	4	LSB	
Differential Nonlinearity	DNL	-2	-	2	LSB	
Gain error	GAIN_E	-0.5	-	0.5	%	

3. IP Block Diagram



4. Foundry & Node

UMC 55nm eFLASH

5. Deliverables

No.	Deliverables	Availability	Note
1	Spec	√	
2	Interface Description & Register Map	√	
3	Layout Frame(.LEF)	√	
4	Top Level Flatten GDS	√	
5	Integration Guideline	√	